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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,814	09/12/2003	Satwant Singh	M-15198 US	7052

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,814	SINGH ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *14-16 and 21-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,17-20 and 32-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed June 23, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13, 17-20, and 32-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Powell (US 5,526,278).

Regarding claim 1, Powell discloses an application specific integrated circuit (ASIC) (col. 1, lines 14+) conversion of a programmable logic device (PLD), wherein the programmable logic device comprises a plurality of PLD logic blocks (col. 15, lines 6+) and a PLD routing structure (col. 15, lines 9+) operable to couple logical inputs to each PLD logic block, comprising:

a plurality of ASIC logic blocks (col. 15, lines 26+) corresponding on a one-to-one basis with the plurality of PLD logic blocks; and

an ASIC routing structure (Fig. 4) configured to couple logical inputs to each ASIC logic block, wherein the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure, and wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure (col. 15, lines 60+).

Regarding claim 2, Lien discloses that the PLD logic blocks and the ASIC logic blocks are lookup table (LUT)-based logic blocks (inherent for FPGA, MPLC, and MPGA).

Regarding claim 3, Lien discloses that the PLD logic blocks and the ASIC logic blocks are programmable AND array-based logic blocks (inherent for FPGA, MPLC, and MPGA to have logic blocks with AND logic array).

Regarding claim 4, Lien discloses that the ASIC includes a plurality of metal layers (col. 15, lines 25+); wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias (inherent) each selected so as to provide either a logic high or a logic low value to the plurality of ASIC logic blocks to provide the same truth tables as used in the PLD logic blocks (col. 12, lines 6+; lines 28+; col. 13, lines 63 - col. 14, lines 48).

Regarding claim 5, Lien discloses that the ASIC includes at least one metal layer, wherein traces formed in the metal layer are customized to provide the same truth tables for the ASIC logic blocks as are used in the PLD logic blocks (col. 12, lines 6+; lines 28+; col. 13, lines 63 - col. 14, lines 48).

Regarding claim 6, Lien discloses that only the first and second metal layers are coupled by vias (inherent) selected so as to provide either a logic high or a logic low value to the plurality of ASIC logic blocks to thereby provide the same truth tables as in the PLD logic blocks (col. 12, lines 6+; lines 28+; col. 13, lines 63 - col. 14, lines 48).

Regarding claim 7, Lien discloses that the first metal layer includes traces carrying voltage levels VCC and VSS, and wherein the vias are selected to couple to VCC to provide a logic high value and to couple to VSS to provide a logic low value (inherent).

Regarding claim 8, Lien discloses that the ASIC includes a plurality of metal layers, and wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias (inherent) each selected so that the coupling provided by the ASIC routing structure routing

structure is the same as that provided by the PLD routing structure (col. 12, lines 6+; lines 28+; col. 13, lines 63 - col. 14, lines 48).

Regarding claim 9, Lien discloses that the PLD routing structure is a buffered, segmented routing structure, each buffered PLD routing segment corresponding to an ASIC buffered routing segment, and wherein the vias are each selected so that the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure on a segment-by-segment basis (col. 12, lines 6+; lines 28+; col. 13, lines 63 - col. 14, lines 48).

Regarding claims 10-13, as for the diode load, channel widths, and inverters, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Claims 17-20 and 32-37 are essentially the same in scope as claims discussed above and are rejected similarly.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER